CAT51DB2 DIGITALLY PROGRAMMABLE POTENTIOMETER (DPP™) DEMONSTRATION BOARD WITH INCREMENTAL UP/DOWN INTERFACE

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1. INTRODUCTION

This document describes the CAT51DB2 Evaluation/Demonstration Board for Catalyst Digitally Programmable Potentiometer (DPP™) ICs with an increment up/down interface. This board gives design engineers a simple way to evaluate digital potentiometers during prototype development. The CAT51DB2 is the second version of the CAT51DB1 board.

The board supports 32-tap (CAT5112/5114) and 100-tap (CAT5111/5113) devices. The series resistor array is between two terminals, R_H and R_L. The wiper, R_W, can be positioned to any of the 32 or 100 positions through an internal up/down counter and decoder. The CAT5111 and CAT5112 have a buffered wiper. All devices feature nonvolatile wiper position memory. Detailed device descriptions and electrical characteristics are in the device data sheets.

2. CAT51DB2 BOARD HARDWARE

The demo board circuits and push button switches generate the U/$\overline{D}$, $\overline{INC}$ and $\overline{CS}$ control signal inputs for the digital potentiometer. The board schematic is shown in Figure 1. Additional information on the demo board operation is available in Design Note 1, “Push-Button Control of Digitally Programmable Potentiometers with an Increment/ Decrement Interface”.

The UP/DOWN switch (S3) controls the direction of the potentiometer wiper. When the switch is set to the up position, the internal counter that sets the wiper position will be incremented. If the switch is set to the down position, the counter decrements and the wiper will move accordingly.

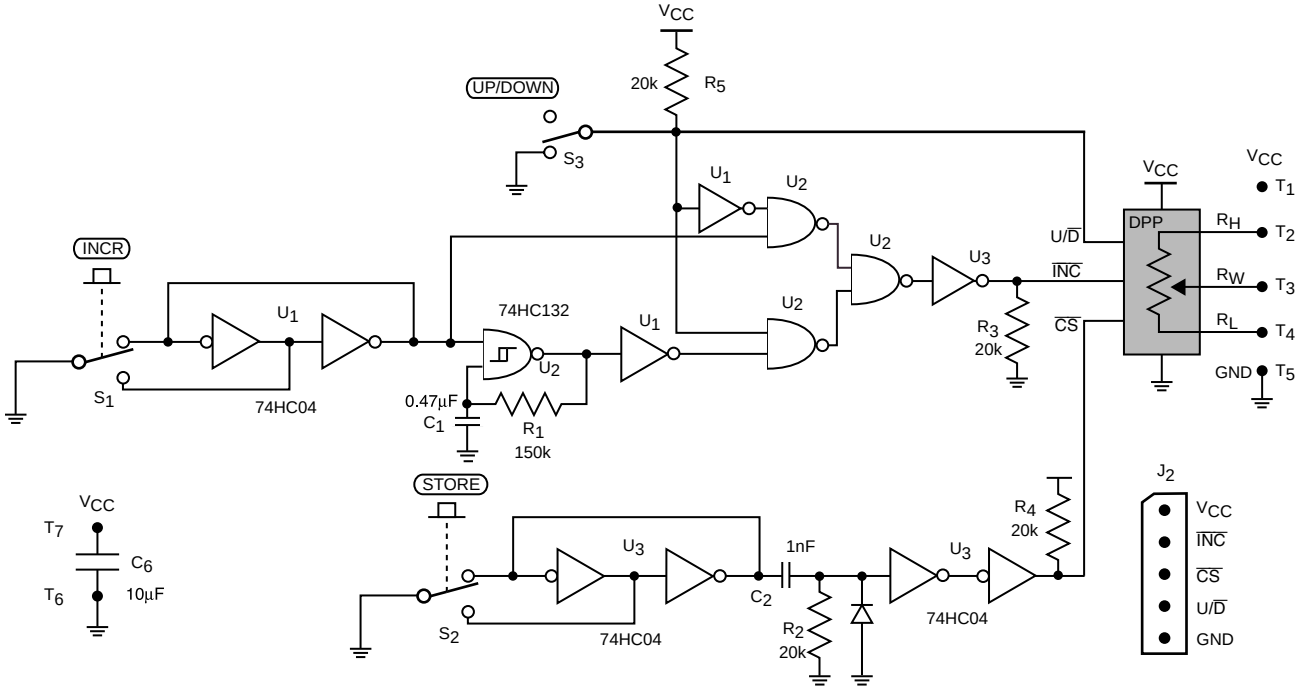

Figure 1. CAT51DB2 Demo Board Schematic

In order to move the potentiometer wiper, a clock pulse is generated at the DPP $\overline{INC}$ input. The INCR push-button switch (S1) enables a low frequency clock. The clock is enabled as long as the INCR switch is pushed.

When S3 is in the "Up" position the counter (wiper) advances on every falling clock edge. For the "Down" position, however,the counter (wiper) is moved only one tap position for every push of the INCR push-button switch.

To store the wiper position in on-chip nonvolatile memory the STORE push button switch (S2) generates a positive pulse at CS. The S1 and S2 switches are debounced.

Table 1 presents the component list for this demo board. The layout of the board is shown in Figure 2.

Table 1. CAT51DB2 Demo Board List of Components

Name	Description	Part #	QTY
R1	Metal Film Resistor 1/16W, 150kohm	Digi-Key 150KXBK-ND	1
R2	Metal Film Resistor 1/16W, 20kohm	Digi-Key 20.0KXBK-ND	1
R3, R4, R5	Metal Film Resistor 1/16W, 20kohm (not critical)	Digi-Key 20.0KXBK-ND	3
C1	Capacitor 0.47µF monolitic ceramic	Panasonic ECU-S1H474MEB (or equiv.)	1
C2	Capacitor 1000pF monolitic ceramic	Panasonic ECU-S2A102KBA (or equiv.)	1
C3, C4, C5	Capacitor 0.022µF monolithic ceramic (decoupling cap)	Panasonic ECU-S2A223KBA (or equiv.)	3
C6	Capacitor 10µF / 10V Tantalum (decoupling cap)	Panasonic ECSF1AE106K (or equiv.)	1
D1	Diode 1N4148	Digi-Key 1N4148MSCT-ND	1
U1	74HC04 Hex Inverter	Digi-Key SN74HC04N	1
U2	74HC132 Quad Schmitt Trigger NAND	Digi-Key MM74HC132N	1
U3	74HC04 Hex Inverter	Digi-Key SN74HC04N	1
U4	8 pin DIP Socket	Digi-Key ED3308-ND	1
DPP	100-Tap Digitally Programmable Potentiometer	Catalyst CAT5113P-00	1
S1, S2	Momentary Contact Switch, SPDT, Vertical Rt. Angle	C&K 8125SD9AV2BE (or equiv.)	2
S3	Toggle Switch, SPDT On-On, Vertical Rt. Angle	C&K E101MD1AV2BE (or equiv.)	1
S4	Slide Switch, SPDT	E-SWITCH EG1218 (or equiv.)	1
T1 to T5	Turret Pin	MILL-MAX 2710-1-00-01-00-00-07-0	5
T6, T7	Header Pins	Digi-Key S1012-02-ND	1
J2	5-pin Header Connector	Digi-Key S1012-05-ND	1
BTH	Attached Battery Holder for 3 AA Cells - PC Mount	Digikey 2464K-ND (Keystone)	1

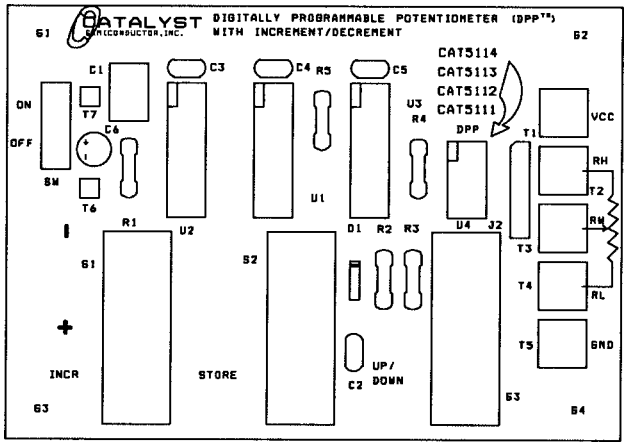

Figure 2. CAT51DB2 Board Layout

The board is powered through an attached battery pack (three 1.5V AA batteries). The power is applied through the SW Slide Switch. The internal power supply voltage that powers the logic and the DPP device can be measured between the T1/ T7 (VCC) and T5/T6 (GND) test points.

3. DPP EVALUATION

All three DPP terminals R_H, R_W and R_L are available through the T2, T3, T4 test points (turret pins). The DPP control inputs ($\overline{INC}$, $\overline{CS}$, U/$\overline{D}$) are available through a 5-pin header connector, J2 (pin #2, #3 and #4). Through the J2 connector, the CAT51DB2 board can be used to control a CAT51xx DPP device in a user application.

The board has an 8-pin DIP socket for the DPP IC (CAT5111, CAT5112, CAT5113 or CAT5114). The board is supplied with a 100kohm, CAT5113-00 device.

The potentiometer functionality can be verified as a variable resistor or as a variable voltage divider. The following steps can be performed to evaluate the DPP device:

1) Power-up the board hardware

Turn the SW switch ON.

2) Potentiometer resistance measurement

The digital potentiometer end-to-end resistance is measured by connecting a DMM (resistance measurement) between the T2 (R_H) and T4 (R_L) test points.

3) Variable resistor evaluation (CAT5114 and CAT5113, unbuffered wiper).

For every push on the INCR momentary contact switch, the variable resistor value will be increased or decreased according to the position of the UP/DOWN switch.

- Connect the DMM (resistance measurement inputs) between the T4 (low-end terminal) and T3 (wiper) test points.
- Press the momentary INCR switch.
- Observe the resistance value measured by the DMM.

4) Non-volatile wiper storage evaluation

The wiper position is stored in nonvolatile memory when $\overline{CS}$ goes from low to high while the $\overline{INC}$ input is high. When power is restored (after a power down), the last stored wiper position is recalled from the nonvolatile memory.

- Using the INCR push button, set the wiper position. Measure the resistance value between T4 and T3.
- Press the STORE push button.
- Momentarily press the INCR button to change the wiper position and measure the variable resistance between T4 and T3.
- Power down the board (SW switch = OFF).
- Power up the board (SW switch = ON).
- Measure the resistance between T4 and T3. The measured value must be the same as the one measured before the STORE operation described above.

5) Variable voltage divider evaluation

- Across the potentiometer terminals T2 and T4 connect an external voltage that is less than or equal to V_{CC}. For example, set T4 equal to GND and T2 equal to 4V.
- Connect a DMM to measure the voltage between T4 (R_L=GND) and T3 (wiper).
- Momentarily press the INCR button.
- Verify the voltage on the wiper terminal.

6) DPP resolution evaluation

To monitor the wiper advance, monitor the DPP $\overline{INC}$ input and wiper terminal using a digital oscilloscope. The wiper moves one position (tap) for every falling clock edge at the $\overline{INC}$ input. The following example applies to the CAT5113-00 (100 taps, Rpot = 100kohm).

- Connect the external voltage, Vext = +4V between the DPP terminals, T2 (R_H) = +4V and T4 (R_L) = GND.
- Connect oscilloscope CH1 to the $\overline{INC}$ input of the DPP device (Pin #1) and oscilloscope CH2 to terminal T3 (wiper).
- Set the initial wiper position using INCR button (i.e. middle position); measure the voltage on wiper terminal T3 (CH2).
- Set the oscilloscope to acquire a single sequence: Trigger CH1, Negative Edge, 50 ms/div, CH1: 2V/div; CH2: 50mV/div (adjust offset); Single Sequence Acquisition.
- Set the Up/Down switch to the Up position.
- Press the INCR push button. The clock pulses applied to the $\overline{INC}$ input of the DPP (CH1) and the wiper voltage (CH2) will be displayed on the oscilloscope screen. (Figure 3).
- Observe the voltage on CH2 relative to the clock pulses on CH1. The voltage on the wiper terminal will increase for every falling clock edge with V_tap = Vext/100 = 4V/100 = 40mV.

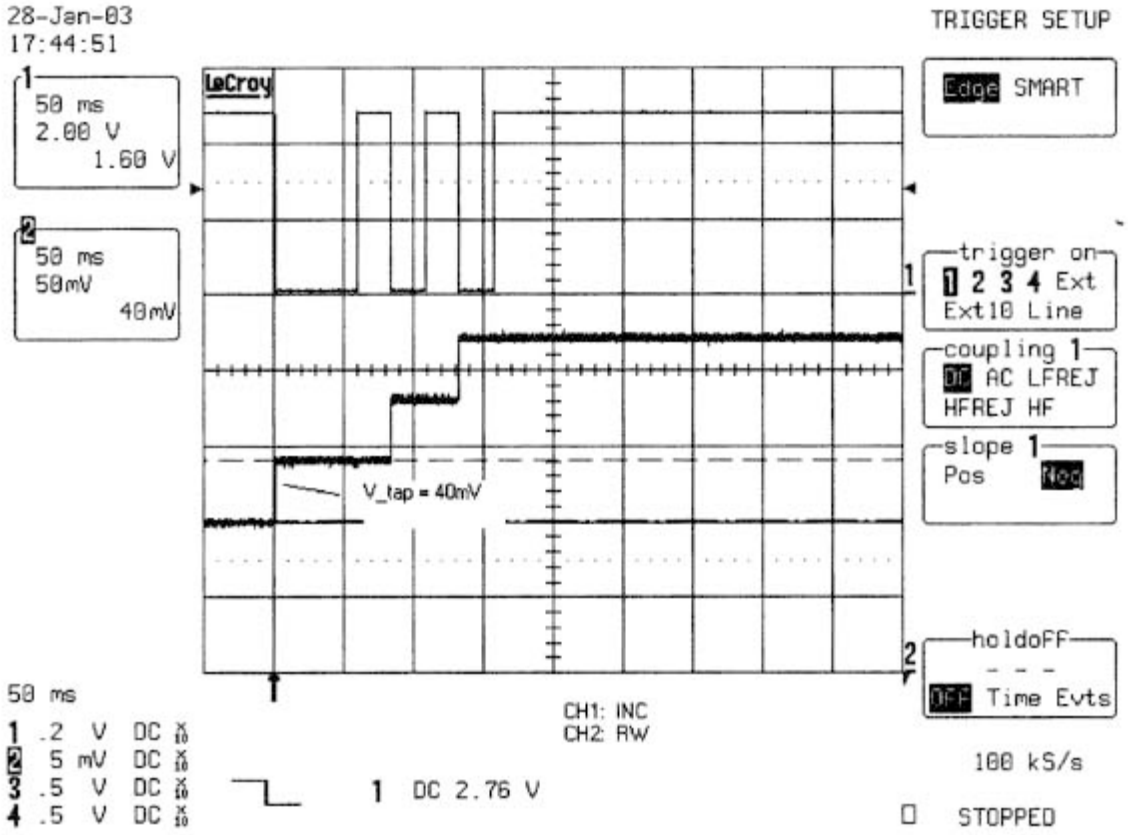

Figure 3. Wiper voltage advances one tap for every negative clock edge

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